|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | | Gate Density   1. Quality of logic - 120 2. Gate 2 - 300 | 420 |  | | Number of Horizontal Layers |  |  | | Number of Vertical Layers |  |  | |  |  |  | | Gate count (excluding memories, macros & subchips) |  |  | | IO area   1. Functional pins - \_\_\_\_100\_\_\_\_ 2. Power Pins- \_\_\_\_\_200\_\_\_\_ | 300 |  | | Memory + Macros + Subchips | Taken from memory list |  | | Target Utilization |  |  | | Additional gate count for CTS, timing closure etc, in percentage |  |  | | Additional gate count for ECOs |  |  | | Linear pad Placement   1. Linear A - 200 2. Linear B - 300 3. Linear c - 100 | 600 |  | | Die size generation constract   1. Die A - 200 2. Die B - 300 3. Die C – 400 4. Die D - 30 5. Die E - 100 | 1030 |  | |